

FIG. 1

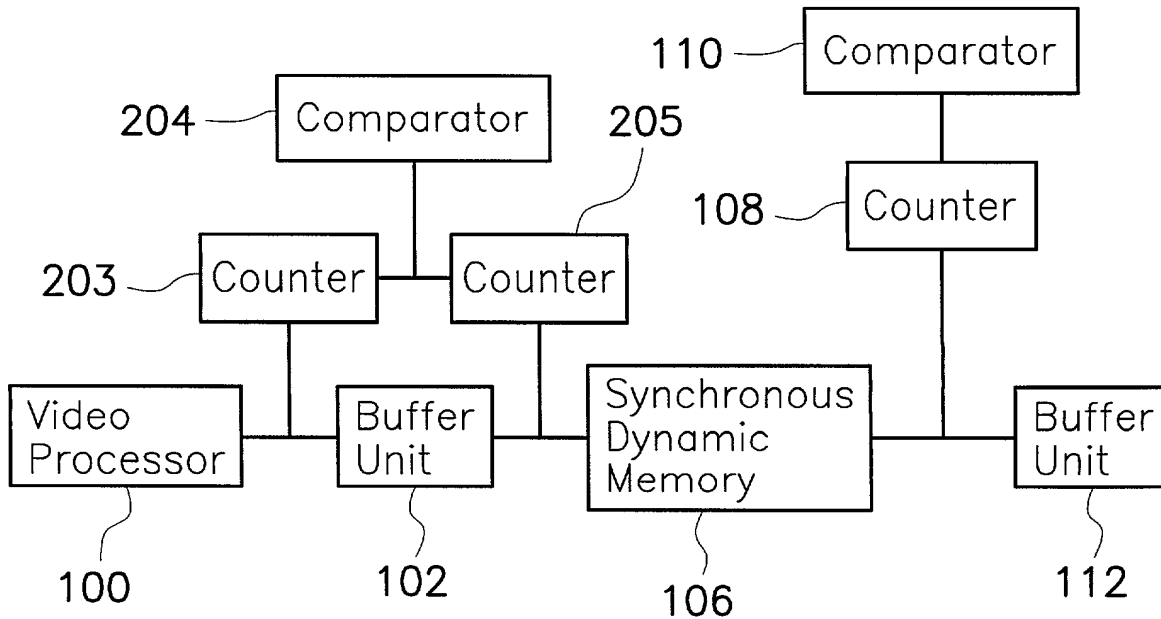


FIG. 2

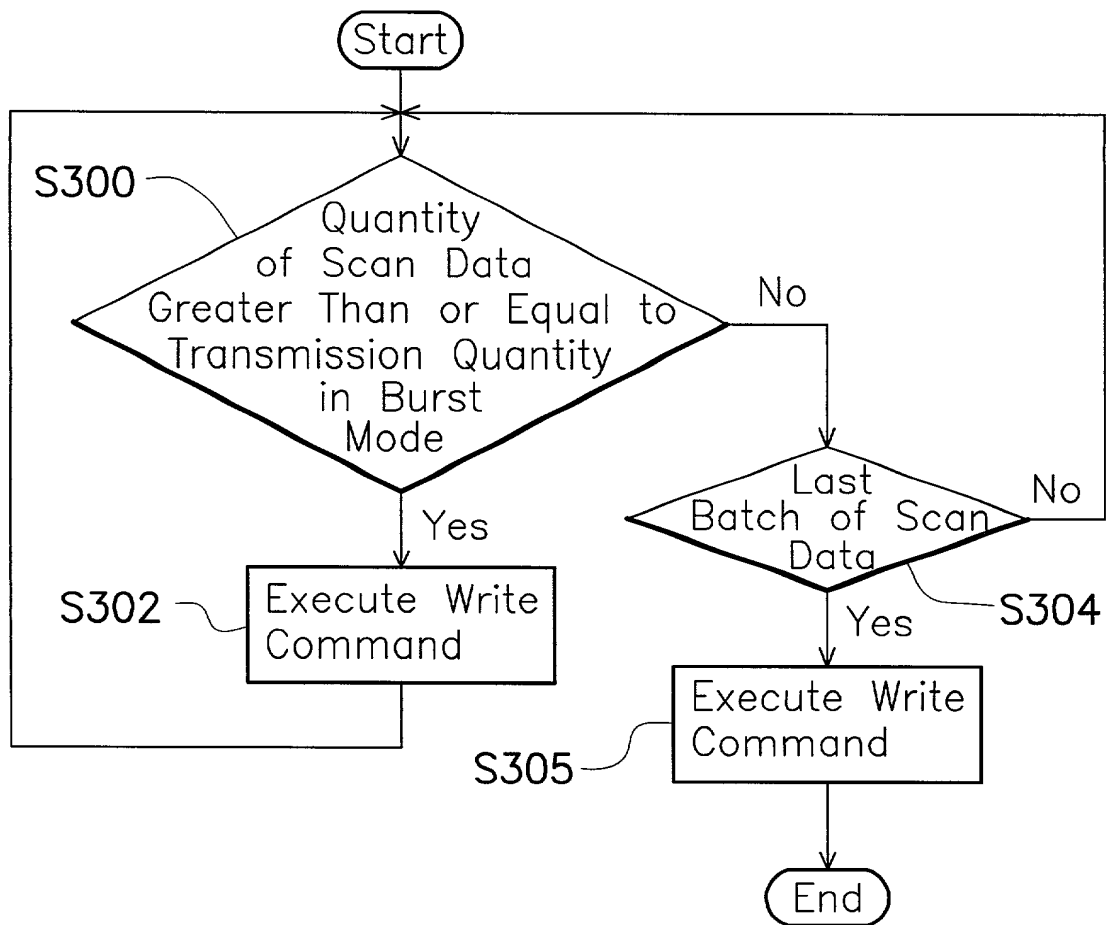


FIG. 3

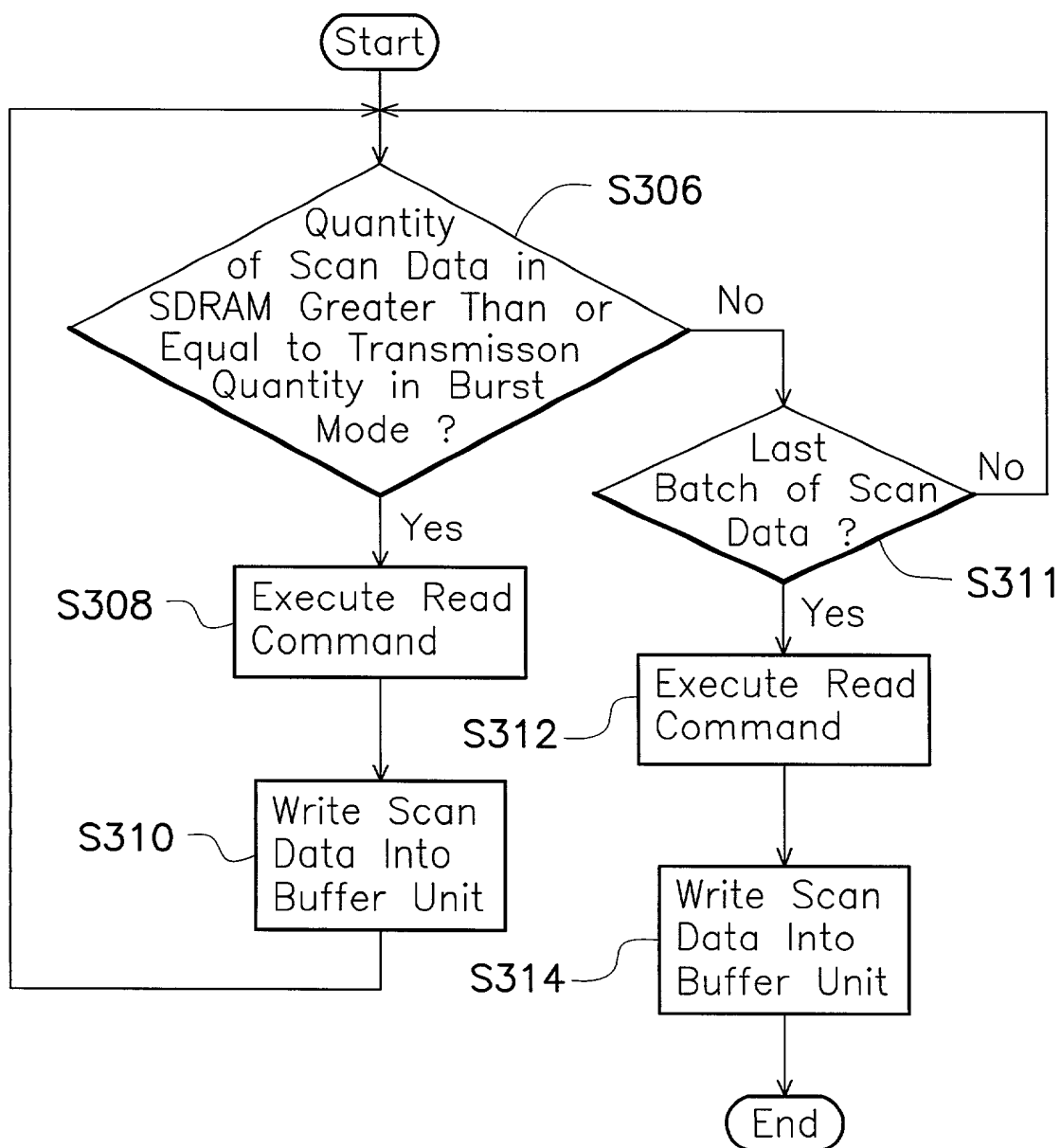


FIG. 4

FIG. 5 is a schematic diagram of a Synchronous Dynamic Memory (SDRAM) array 106. The array is organized as a 4x1 grid of memory cells. The cells are numbered 1, 2, 3, and 4 from top to bottom. A TAG (Tag) is associated with the array, pointing to the third cell (3). The TAG is labeled 400. The array is labeled 402.

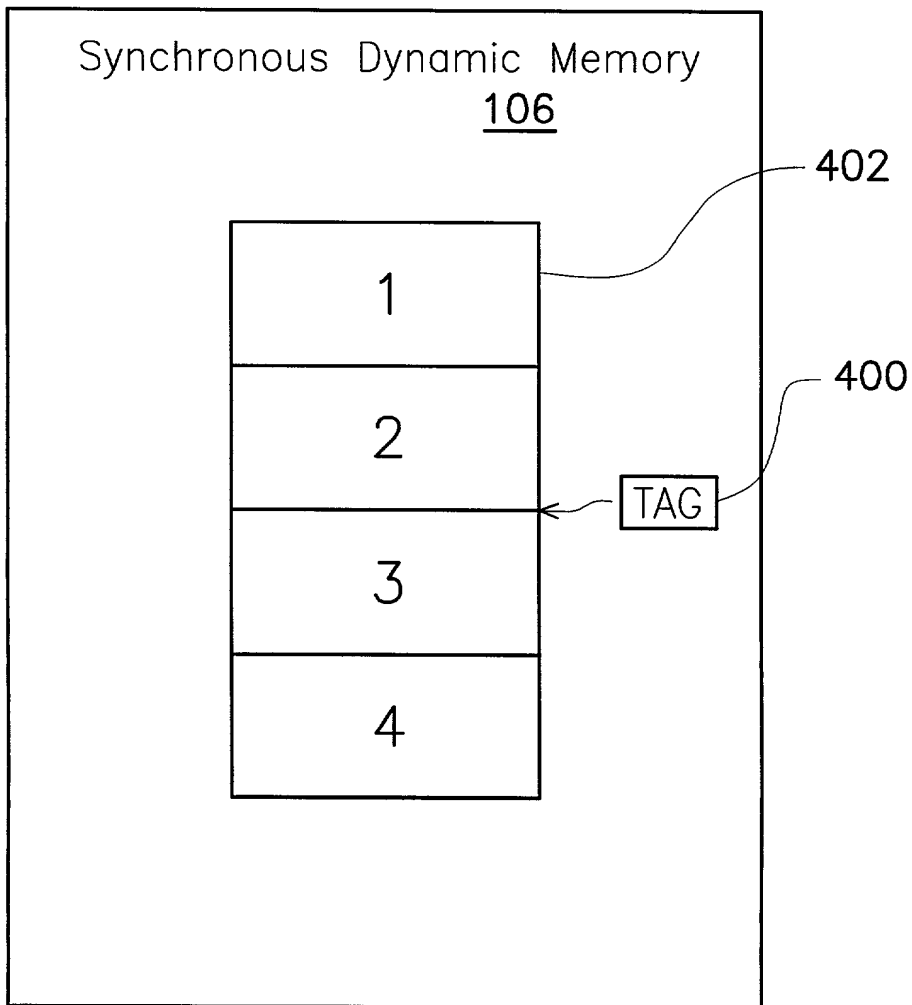


FIG. 5